WHAT IS CLAIMED IS:

1. A semiconductor device manufacturing method comprising the steps of:

(a) preparing a semiconductor substrate;

(b) forming, on said semiconductor substrate, a first insulation film where a first interconnect with a copper-based first conductor film and a capacitor bottom electrode are buried;

(c) forming a second insulation film on said first insulation film where said first interconnect and said bottom electrode are buried;

(d) forming a third insulation film on said second insulation film;

(e) forming a first hole by removing a selected area of said third insulation film;

(f) forming a capacitor top electrode with a second conductor film in said first hole;

(g) forming a fourth insulation film on said third insulation film where said top electrode is buried;

(h) forming a second hole and a third hole to expose said top electrode by removing a selected area of said fourth insulation film, and forming a fourth hole to expose said first interconnect by removing selected areas of said third insulation film and said second insulation film at the bottom of said second hole; and

(i) filling a copper-based third conductor film into said second hole, said third hole, and said fourth hole.

2. The semiconductor device manufacturing method according to Claim 1, wherein said second insulation film suppresses or prevents diffusion of copper.

3. The semiconductor device manufacturing method according to Claim 1, wherein said second insulation film lying between said bottom electrode and said top electrode functions as a capacity insulation film for a capacitor.

4. The semiconductor device manufacturing method according to Claim 1, wherein, at said step (e), a first hole is made by removing selected areas of said third insulation film and said second insulation film,

after said step (e) and before said step (f), further comprising the step of:

(e1) forming a fifth insulation film on said third insulation film including the bottom and side walls of said first hole.

5. The semiconductor device manufacturing method according to Claim 4, wherein said fifth insulation film lying between

said bottom electrode and said top electrode functions as a capacity insulation film for said capacitor.

6. The semiconductor device manufacturing method according to Claim 1, wherein:

at said step (e), a plurality of said first holes are made;

at said step (f), said top electrode is formed in each of said plural first holes; and

at said step (h), said third hole exposes said top electrode formed in each of said plural first holes at its bottom.

7. The semiconductor device manufacturing method according to Claim 1,

said step (b) comprising the sub-steps of:

(b1) forming said first insulation film on said semiconductor substrate;

(b2) forming a fifth hole and a sixth hole in said first insulation film;

(b3) forming said copper based first conductor film which fills said fifth hole and said sixth hole; and

(b4) forming said first interconnect inside said fifth hole and said bottom electrode inside said sixth hole

by removing said first conductor film except its part buried in said fifth hole and said sixth hole.

8. The semiconductor device manufacturing method according to Claim 1,

said step (f) comprising the sub-steps of:

(f1) forming said copper based second conductor film which fills said first hole; and

(f2) forming said top electrode inside said first hole by removing said second conductor film except its part buried in said first hole.

9. The semiconductor device manufacturing method according to Claim 1, after said step (i), further comprising the step of:

(j) removing said third conductor film except its parts buried in said second hole, said third hole, and said fourth hole.

10. The semiconductor device manufacturing method according to Claim 9, wherein at said step (j), said third conductor film buried inside said second hole and said fourth hole constitutes a second interconnect electrically connected with said first interconnect, and said third conductor film

buried inside said third hole constitutes a conductor area electrically connected with said top electrode.